Remarks:

Applicants appreciatively acknowledge the Examiner's confirmation of receipt of Applicants' claim for priority and certified priority document under 35 U.S.C. § 119(a)-(d).

Reconsideration of the application, as amended herein, is respectfully requested.

Claims 1 - 8 are presently pending in the application. Claims 1, 5 and 6 have been amended. New claims 7 - 8 have been added. The amendments to claims 1, 5 and 6 are supported by the specification of the instant application, for example, on page 7, line 15 - page 8, line 2 and col. 2, lines 16 - 24. New claims 7 and 8 are additionally supported by the specification of the instant application, for example, on page 10, lines 5 - 7 (i.e., claim 7) and page 5, lines 10 - 13 (i.e., claim 8).

In item 1 of the above-identified Office Action, claims 1 - 6 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by U. S. Patent No. 6,000,048 to Krishna et al ("**KRISHNA**").

Applicants respectfully traverse the above rejections, as applied to the amended claims.

More particularly, claim 1 recites, among other limitations:

> **a microcontroller connected to said external access terminal and to said memory, said microcontroller controlling an access to said memory and a data transfer through said external access terminal <u>during normal operation</u>, said microcontroller controlling a performance of a test sequence for functional testing said memory in a test operation of the module;** and
>
> **a defect data memory for storing addresses of the memory cells of said memory which have been detected as defective, said addresses being generated during the functional testing.** [emphasis added by Applicant]

As such, Applicants' claim 1 requires, among other things, a microcontroller for controlling, **during normal operation of the module**, an access to the memory and a data transfer via the external terminal of the module, **which microcontroller is additionally used to perform functional testing of the memory.** Using the module's existing microcontroller (i.e., the microcontroller **already present** for the normal operation of the module) to perform the test operation of the module makes it possible to dispense with BIST hardware on the module. As a result of Applicants' invention of claim 1, valuable chip area can be saved. This is particularly advantageous with regard to modules having a high integration density. See, page 6 of the instant application, lines 8 - 12.

However, contrary to Applicant's claimed invention, the **KRISHNA** reference discloses a combined logic and memory circuit with built-in memory test, **which requires additional**

circuitry to be added to the IC just to test the DRAM. See, the Abstract of **KRISHNA** ("Additional logic circuitry is included within the IC to enable the IC to test the DRAM, that is, a built-in self test of the DRAM."). **KRISHNA** discloses that it is expected ("though not required") that this additional circuitry (including a controller) will be used **exclusively** for performing the BIST functions. For example, col. 9 of **KRISHNA**, lines 42 - 45, states:

> It is expected, though not required, that most if not all of the **control unit 74**, the instruction register 56, the program counter 88, and the tester register 92 **will be used exclusively for the BIST functions.** [emphasis added by Applicants]

KRISHN certainly does not teach or suggest doing away with the BIST controller and using the controller that performs normal operations on the IC to additionally perform BIST functions. Even, by stating the caveat (i.e., "It is expected, though not required") **KRISHNA** is merely suggesting that the BIST circuitry be provided, but need not be used exclusively for the BIST functions. This statement in **KRISHNA** is in no way a teaching or a suggestion to do away with the **BIST controller, in order to use the normal microcontroller of the IC to perform BIST functions.**

In fact, it is a goal of **KRISHNA** to expand the BIST circuitry to specifically include the BIST controller. Col. 4 of **KRISHNA**, lines 4 - 6, state:

> The logic section <u>is expanded to include</u> a **microcontroller for built-in self testing (BIST)** that executes BIST instructions stored by the logic tester in the secondary memory so as to test the larger primary memory. [emphasis added by Applicants]

Modifying **KRISHNA** in order to make the invention of Applicants' claim 1 (i.e., omitting the BIST microcontroller and having those functions performed by the IC's regular microcontroller) would destroy the teachings of **KRISHNA** (i.e., those of **expanding** the logic section to include a BIST controller). As such, the **KRISHNA** reference fails to teach or suggest Applicants' invention of claim 1 and cannot be modified to teach or suggest Applicants' invention of claim 1 without impermissibly destroying the teachings of the **KRISHNA** reference.

As such, it is believed that, among other limitations of Applicants' claim 1, **KRISHNA** does not, and cannot, teach or suggest using the same microcontroller on the IC that controls data transfers **during normal operation**, as the BIST controller. As such, it is believed that Applicants' invention of claim 1 is patentable over **KRISHNA**.

Further, Applicants' amended claim 1 recites, among other limitations:

> **a defect data memory for storing addresses of the memory cells of said memory which have been detected as defective**, said addresses being generated during the functional testing. [emphasis added by Applicants]

Applicants' claim 5 has been similarly amended to recite, among other limitations:

> **storing addresses of memory cells of the memory which have been detected as defective** during the functional testing **in a defect data memory** under the control of the microcontroller. [emphasis added by Applicants]

As such, all of Applicants' claims require, among other things, that the addresses of the defective memory cells be stored in a defect data memory. The addresses of the defective memory cells are stored in a defect data memory in the claimed invention so they can then be used to construct a fail bit map, as described in the specification of the instant application, page 6, lines 12 - 15, which states:

> The respective defect data can be read out by an external test unit at the end of the functional test and may serve in particular as a basis for constructing a fail bit map. [emphasis added by Applicants]

Additionally, the addresses of the defective memory cells can be used to form a defect table from which the fail bit map is

produced, in order to replace the memory cells with defect-free redundant memory cells, as disclosed in the specification of the instant application, for example, on page 2, lines 15 - 23, which states:

> **To that end, the addresses of the tested memory cells which have been detected as defective are stored in a defect address memory to form a so-called defect table** in order to replace the memory cells by defect-free redundant memory cells in a subsequent step on the basis of the stored addresses. **On the basis of the defect table**, the repair solution specific to each memory can subsequently be calculated and **a so-called fail bit map can be produced.** [emphasis added by Applicants]

However, it is not possible in **KRISHNA** to store addresses of defective memory cells during the functional testing. Rather, **KRISHNA** only discloses providing **an 8-bit test register 92**, to provide control information and receive the testing status and results. The format of the 8-bit test register 92 of **KRISHNA** is illustrated in Table 1 of **KRISHNA**, reproduced herebelow for convenience.

TABLE 1

BIT POSITION	BIT FUNCTION
1	START
2	STATUS
3	TEST_RESULT
4	
5	
6	
7	
8	

Information is stored in the 8-bit test register of **KRISHNA** as described in col. 6 of **KRISHNA**, lines 16 - 37, which states:

> **The first bit START can be stored with a value that instructs the BIST control unit 78 that the built-in self test should start immediately.** The START bit is set by the VLSI tester to initiate immediate testing and is reset by the BIST control unit 78 when the built-in self test has been completed. **The second bit STATUS is set by the BIST control unit 78 at the beginning of the self test, and is reset by the BIST control unit 78 at the end of testing.** Its primary function is to lock out the PCI bus from rewriting during BIST testing any of the DRAM or SRAM memory locations or any registers in the combined logic/BIST section 54 that are relevant to BIST. In particular, it prevents a second invocation of BIST from interfering with an ongoing BIST. **The third bit contains the result TEST RESULT of the built-in self testing. In its simplest implementation, one bit describes whether no error was found or whether at least one error was found during the built-in self test. The number of bits for TEST RESULT could be expanded to indicate the number of errors or type of error detected in the DRAM.** The STATUS and TEST_RESULT bits should be read-only to the VLSI tester since only the BIST control unit 78 should change them. [emphasis added by Applicants]

As can be seen from the forgoing, the 8-bit test register disclosed in **KRISHNA** neither teaches, nor suggests, **storing the addresses of defective memory cells therein**, nor is it possible **to store the addresses of the defective memory cells in the 8-bit test register of KRISHNA.** Nowhere in **KRISHNA** is it taught or suggested to provide a defect data memory, as recited by all of Applicants' claims, in which the addresses of the defective memory cells, detected during the functional testing, are stored.

Since it is not taught or suggested in **KRISHNA**, nor even possible, to store the **addresses** of defective memory cells found during functional testing in a defect data memory, as required by Applicants' claims, Applicants' claims are believed to be patentable over the **KRISHNA** reference.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claims 1 and 5. Claims 1 and 5 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1 or 5.

In view of the foregoing, reconsideration and allowance of claims 1 - 8 are solicited.

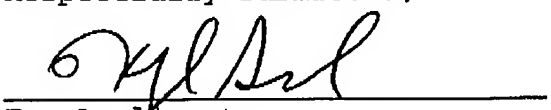
In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

If an extension of time for this paper is required, petition for extension is herewith made.

Applic. No. 10/616,114
Response Dated June 12, 2006
Responsive to Office Action of March 10, 2006

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,



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